Synthesis of ultra-dense interferometric chains in planar lightwave circuits

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ABSTRACT

Planar lightwave circuits (PLCs) provide economical, high-capacity solutions for systems using wavelength-division multiplexing. To accommodate a higher volume of optical integration in a smaller footprint, PLC technology has trended towards higher refractive index contrast platforms resulting in tighter optical confinement. Further progress in the densification of photonic functionality, especially for multi-stage interferometric configurations, must rely on the development of advanced architectures to increase the density of functional units. We present a breakthrough approach to the synthesis of ultra-dense interferometric chains, reaching packing density of waveguides close to theoretical limits. The proposed framework is well suited for mixed parallel and sequential interferometric structures in low- or high-refractive index contrast platforms. The new methodology allows the addition of stages to an interferometric chain without appreciable increase in device footprint, thus creating a highly-optimized ultra-dense waveguide layout. To validate this approach, we designed and fabricated a 4-λ LAN multiplexer that comprises 7 interferometric stages in a silica-on-silicon platform with a refractive index contract of Δn = 2.0%. Despite the relatively low refractive index contrast, the device was realized in a footprint of only 0.15 cm^2. The multiplexer exhibits exceptional optical performance, including on-chip loss of 0.2 dB, negligible polarization-dependent loss, and a remarkably flat single-mode spectral response with no insertion loss penalty. This ultra-compact implementation, combined with the state-of-the-art optical performance characteristics, led to a wide deployment of the multiplexer in data center applications, and provided a rapidly-advancing roadmap for unprecedented densification of optical functionality in PLCs in any refractive index platform.

Keywords: planar lightwave circuit, silica-on-silicon, densification, integrated optics, interferometric, multiplexer, waveguides, LAN

1. INTRODUCTION

Over the past three decades, planar lightwave circuits (PLCs) have evolved to become key functional and integration blocks in many applications, including optical communication systems, sensing, medical devices, spectroscopy, lidar, atomic clocks, and RF signal processing. PLCs provide economical, high-capacity solutions for systems that exploit spectral properties of light or rely on wavelength-division multiplexing (WDM). Coherent optics enabled by PLCs allows the separation of signals not only by wavelength and amplitude, but also by phase and polarization.

The number of subcomponents in integrated PLCs has grown consistently over the years. To accommodate a higher density of optical integration, the PLC technology has trended towards higher refractive index contrast platforms. The higher index contrast results in tighter optical confinement, which allows smaller bend radii, and thus more functionality in the same footprint. Most notable among these platforms are silicon-on-insulator (SOI),[1] III-V photonics,[2] and silicon nitride (Si_3N_4).[3]

This approach towards smaller radii of curvature in the photonics industry is reminiscent of the reduction of the transistor size in the electronics industry, which has resulted in doubling of the number of transistors in an integrated circuit (IC) every two years over the past half century. However, there are significant differences between these two technological progressions. First, the confinement of electrons in an IC can be achieved on a nanometer scale, whereas the confinement of photons in a PLC is commensurable with the wavelength of photons and is typically on a scale of a micron. This has led, for example, to the dominance of the separate-confinement-heterostructure for building laser diodes, where the confinement of electrons is done separately from the confinement of photons. The second significant difference relates to the limiting factor for increasing the density of components. In ICs, the ability to pack electronic components is limited by lithography, yet lithography is not a limiting factor in PLCs, where much larger waveguide geometry is necessary for light confinement. Bend radii as small as 3-μm have been demonstrated in silicon waveguides

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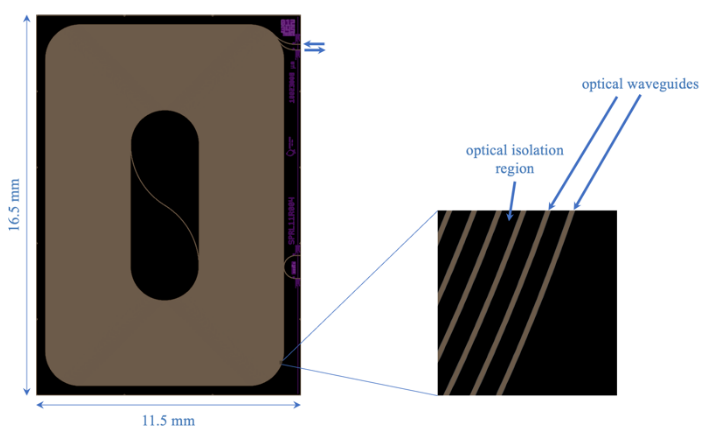
with ultra-high optical confinement, yet the lithographic features that are needed to achieve this limit remain orders of magnitude larger than typically deployed in ICs.[4] Thus it is important to realize that the limiting factor for increasing the density of optical components is architectural in nature. In a typical PLC, the ratio of the area of active waveguides to the total area of the chip remains very small, primarily due to the subcomponent packing limitations of traditional architectures.

In this paper, we present a scalable architecture that enables a compact arrangement of arbitrarily-long interferometric structures. We demonstrate that the synthesis of ultra-dense interferometric chains can be done in a way that achieves waveguide packing density close to theoretical limits, and allows the realization of compact devices regardless of whether a high or low refractive index contrast platform is used. The proposed methodology is able to synthesize Mach-Zehnder interferometer (MZI) structures in such a way that each additional stage of the interferometer can be added without a significant increase in the device footprint. To validate this approach, we have designed and fabricated a 4-λ LAN multiplexer that comprises 7 asymmetric MZI structures in a silica-on-silicon platform with a refractive index contrast of $\Delta n = 2.0\%$. Despite this relatively low refractive index contrast, the device was realized in a footprint of only 0.15 cm^2. The multiplexer possesses state-of-the-art insertion loss, passband flatness, and polarization-invariance characteristics that allow the chip to be widely deployed commercially.

2. DESIGN ARCHITECTURE

2.1 Proposed architecture

The maximum density of the waveguides in a PLC chip is limited by the optical isolation distance that prevents undesirable coupling between the waveguides. Figure 1(a) shows an example of a chip that has the waveguide density close to the theoretical limit for the confinement factor used. The chip was fabricated in silica-on-silicon with a refractive index contrast of $\Delta n = 2.0\%$. The area of the chip is 1.9 cm^2 and the physical length of the waveguide in the coil is 10 meters. Figure 1(b) shows the transmission spectra of such a coil, in TE and TM polarizations, indicating that the propagation loss is 0.01 dB/cm and that the chip does not have a significant source of polarization dependent loss.



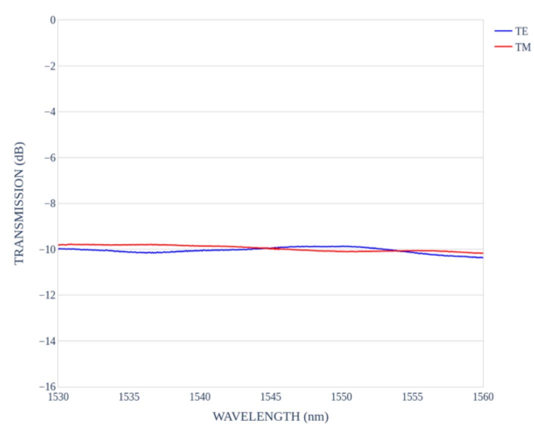


Figure 1. (a) Layout of a 10-meter long coil, fabricated in a silica-on-silicon platform with $\Delta n = 2.0\%$ refractive index contrast and a footprint of 1.9 cm^2. (b) Transmission spectra of the 10-meter long coil, with propagation losses of 0.01 dB/cm and negligible polarization dependent loss.

WDM systems that are based on cascaded multi-stage MZI structures typically require a large footprint due to the serial nature of the interferometers, with each subsequent stage of the interferometer relying on the optical response from the preceding stage. Various approaches have been undertaken for folding the interferometric chains, with zig-zag patterns most commonly used.[5-6] However, as the number of interferometers increases, the physical dimensions of the chip inevitably increase.

The key element of the proposed architecture is a generalized coil pattern shown in Figure 1, which serves as a basis for the waveguide layout with a high density of interferometric structures. Figure 2 shows an example of this approach, where the bent regions of the coil are interspersed with straight regions. The bends of the coil are used to create a natural phase delay between the adjacent waveguides due to the outer waveguide being longer than the inner waveguide. In fact, by adjusting the shapes of the waveguides, one can achieve arbitrary delays between adjacent waveguides. The straight sections of the coil are used to produce the desired amount of coupling between adjacent waveguides.

A half-turn through the coil contains two straight sections and one bend, effectively allowing for a single MZI structure to be implemented. The incremental cost of adding an additional interferometric stage is very low because the footprint of the chip increases only by the area between adjacent bent waveguides of the added interferometric stage. The excess insertion loss, which corresponds to a loss through a 180° section of the coil, is also very small.

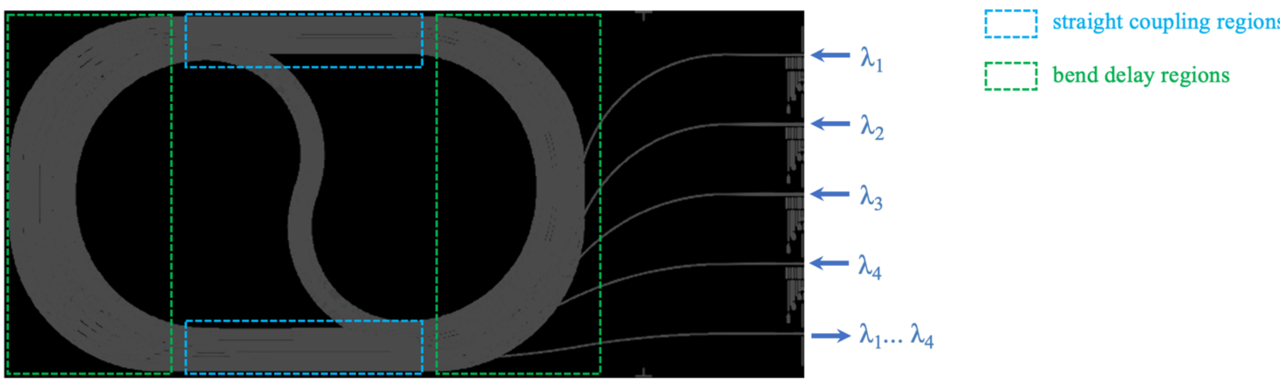


Figure 2. Layout of a 4-λ LAN multiplexer in a silica-on-silicon platform with Δn = 2.0% refractive index contrast and a footprint of 0.15 cm^2.

2.2 Mathematical construction

In order to construct the delay lines, we follow the center-line of the underlying coil. All bent waveguides forming the delay lines are built using cubic Bézier curves of the following parameterized form ($0 \le t \le 1$):

$$S(t) = (1-t)^3 P_0 + 3(1-t)^2 t P_1 + 3(1-t)t^2 P_2 + t^3 P_3 \tag{1}$$

Here, P_0 and P_3 represent the start and end points of the waveguides, whereas P_1 and P_2 are chosen symmetrically relative to the horizontal axis running through the middle of the device. In practice, each Bézier curve is split into two symmetrical sections using the de Casteljau algorithm.[7] The optical delay is then achieved through the optimization of the physical length difference ΔL between the two adjacent waveguides by using point P_1 as a parameter. Point P_2 is then constructed symmetrically.

We use numerical quadrature to compute the lengths of the cubic Bézier curves. It is important that the reciprocal of the radius of the osculating circle $K(t)$ always stays below the critical value K_{max} at which the propagation loss through the curve becomes detectable. To achieve this, we impose a constraint on equation (1) in the form of:

$$K(t) = \frac{\left\| S'(t) \times S''(t) \right\|}{\left\| S'(t) \right\|^3} \le K_{\max} \tag{2}$$

In the straight sections of the coil, the construction of the couplers is fairly straightforward as the amount of coupling can be controlled through the length of the coupling region.

3. 4-λ LAN-WDM MULTIPLEXER

In order to validate our approach, we have selected a relatively low index contrast silica-on-silicon PLC platform to construct a 4 channel LAN-WDM multiplexer. High performance 4-λ LAN-WDM multiplexers have sparked research interest due to their key role in achieving both 800GbE and 1.5TbE Ethernet transmission standards,[8] with demonstrated transmission speeds as high as 225 Gbps/λ.[9]

To fabricate the multiplexer, we used a silica-on-silicon platform with a refractive index contrast of $\Delta n = 2.0\%$ and waveguide dimensions of 3.0×3.0 μm. The devices were realized using a combination of atmospheric pressure chemical-vapor deposition and reactive ion etching. The length of the waveguide does not make a significant contribution to the device performance due to very low propagation losses of silica waveguides (< 1 dB/m, as shown in Figure 1). However, the relatively low refractive index contrast restricts the maximum curvature to $K_{\max} = 1/1000\ \mu\text{m}^{-1}$.

Figure 3 shows a photograph of the fabricated chip, which realizes the multiplexer using the conceptual layout of curved and straight sections shown in Figure 2. The size of the chip is only 0.26×0.57 cm, corresponding to a footprint area of 0.15 cm^2 , and it incorporates a total of seven MZIs. The functionality of the multiplexer and the choice of design parameters replicate a binary tree of cascaded MZI lattice filters that are described in detail elsewhere[10] for an 8-channel device. As shown in Figure 4, we only utilize the first two stages of the described architecture because our multiplexer is a 4 channel device.

Figure 3. Photograph of a 4-λ LAN-WDM multiplexer chip, fabricated in silica-on-silicon with a refractive index contrast of $\Delta n = 2.0\%$ and a footprint of 0.15 cm^2.

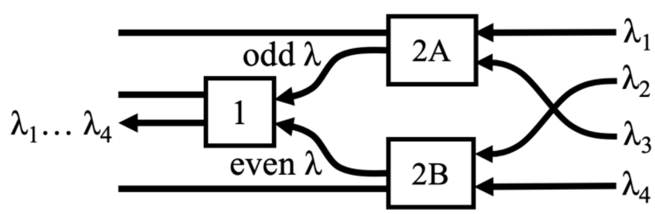


Figure 4.

Figure 4. Schematic of a 4-to-1 multiplexer based on a binary tree of filters.

For our fabricated multiplexer devices, the base length difference, as defined by Horst et al.[10], is $\Delta L_{\text{base}} = \lambda^2 / (2\, \delta\lambda\, n_{\text{gr}}) =$ 120.144 μm, where n_{gr} is the group index. A shift of one full FSR is achieved by adding a delay line length difference of $\Delta L_{\text{FS}} = \lambda / n_{\text{eff}} = 0.888$ μm, where n_{eff} is the effective index of the waveguide. Table 1 shows the delays of each of the stages of the MZI chain shown in Figure 4.

Table 1. Parameters for the calculation of the delay line lengths in the cascaded MZI filters used to construct the multiplexer.

Stage	Delay line lengths
1	ΔL_{base} $\Delta L_{\mathrm{base}}/2$ $\Delta L_{\mathrm{base}}/2 + \Delta L_{\mathrm{FS}}$
2A	$\Delta L_{\mathrm{base}}/2$ ΔL_{base}
2B	$\Delta L_{\mathrm{base}}/2 + 3/4\ \Delta L_{\mathrm{FS}}$ $\Delta L_{\mathrm{base}} + 3/2\ \Delta L_{\mathrm{FS}}$

Figure 5 shows the transmission spectra of a fiber pigtailed 4-λ LAN-WDM multiplexer, for TE and TM polarized light. The device exhibits worst channel insertion loss of 1.4 dB. Most of the insertion loss is due to two fiber couplings with on-chip loss estimated at 0.2 dB. A single-mode spectral response of each channel is flat with a 1-dB bandwidth of 3.6 nm (greater than 80% of the channel pitch). The worst case adjacent crosstalk is 18 dB. The device operates independently of polarization with a polarization dependent loss of less than 0.2 dB.

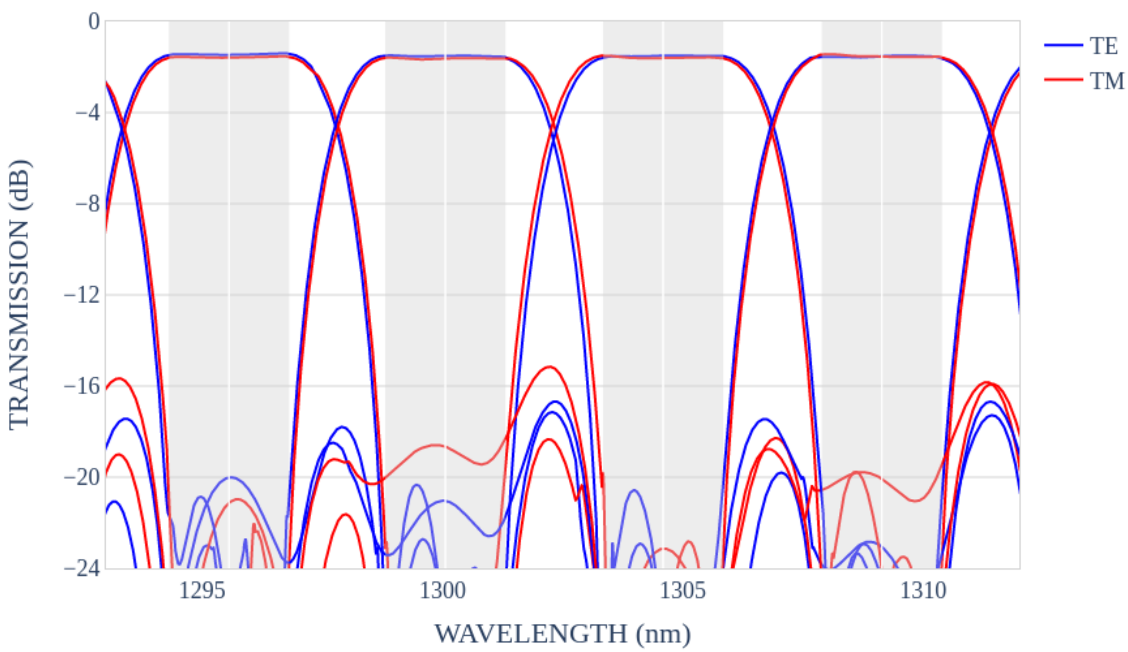


Figure 5. Measured transmission spectra of a 4-λ LAN-WDM multiplexer, including two fiber coupling. The on-chip loss is estimated at 0.2 dB with a 1-dB bandwidth of 3.6 nm.

In addition to its high optical performance characteristics, the multiplexer has proven to be remarkably robust in volume manufacturing, resulting in its large-scale deployments in data center applications. The proposed synthesis of the interferometric chains is easily scalable to a greater number of channels and/or MZI chains that comprise a large number of stages, and has become a backbone for a wide family of ultra-dense photonic chips currently under development.

4. CONCLUSIONS

Further progress in the densification of photonic functionality must rely on the development of advanced architectures that facilitate optimal packing of optical subcomponents. We proposed a methodology to synthesize arbitrary-length interferometric chains in a small footprint for high and low refractive index contrast platforms. We validated our approach by designing and fabricating a 4-λ LAN multiplexer that comprises 7 asymmetric MZI structures in a silica-on-silicon platform with a refractive index contrast of $\Delta n = 2.0\%$. Despite the relatively low refractive index contrast, the footprint of the device was only 0.15 cm^2. The multiplexer possesses state-of-the-art optical performance characteristics that led to its wide deployments in data center applications. The proposed synthesis of the interferometric devices can be readily scaled to a large number of channels and long interferometric chains.

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