Photonic integrated circuits based on silica and polymer PLC

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ABSTRACT

Various methods of hybrid integration of photonic circuits are discussed focusing on merits and challenges. Material platforms discussed in this report are mainly polymer and silica. We categorize the hybridization methods using silica and polymer waveguides into two types, chip-to-chip and on-chip integration. General reviews of these hybridization technologies from the past works are reviewed. An example for each method is discussed in details. We also discuss current status of our silica PLC hybrid integration technology.

Keywords: Photonic integrated circuits, planar lightwave circuits, hybrid integration, waveguide, polymer, silica

1. INTRODUCTION

Optical network has been supporting exponential growth of internet driven communication capacity. The traffic in the network is constantly growing last two decades[1]. The key element for the sustainable growth is the development of optical devices used in the network. The market demands lower cost, higher performance devices. To accommodate these needs, optical devices used in the network have evolved from bulk optics or micro-optics assembled systems to highly integrated systems.

We have developed, over the years, silica and polymer based waveguides technologies (PLCs or PICs). These material platforms have advantages and challenges. For example, silica has very low propagation loss, but to tune the index it requires a high temperature, i.e. power. On the other hand, polymer can have much lower power requirements for index tuning, but it generally has higher propagation loss. Naturally, combination of these materials could provide both lower propagation loss and lower power consumption compared to single material system.

Here, we discuss hybridization in two categories. First we review the general concept of each type. Then we discuss the examples we demonstrated. We also discuss our current work on silica PLC hybridization with passive and active components, not including polymer.

2. SILICA AND POLYMER PLC HYBRIDIZATION

2.1 Types of hybridization

Polymer and silica integration has been proposed and demonstrated by a number of researches. We can categorize the methods used into two types. In the first type, the waveguides are fabricated in the each material and then these circuits are coupled together. The waveguide circuits are complete in each material/chip and functional. In another word, the circuits could work if we separate these chips. The integration here is intended to reduce the cost in material and processes, to scale the production volume, and, in some cases, to realize a new function. The second type is to form a waveguide circuit (or other function) using the both materials together. In this case, the circuit won't work if we separate the materials. Figure 1 shows schematic view of these two types of hybridization. Let's call (a) type chip-to-chip integration, and (b) type on-chip integration in this report.

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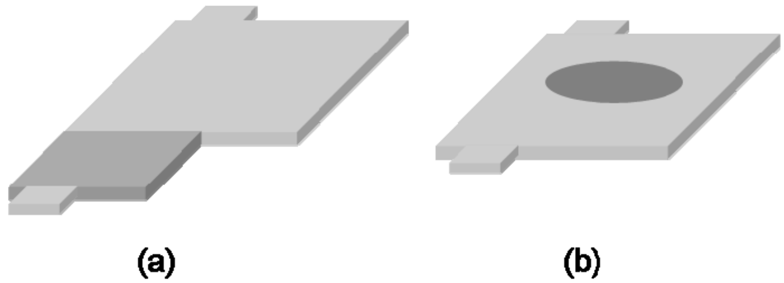

Figure 1. Schematic diagrams of two types of hybrid integrations. (a) Chip-to-chip integration. Separate chips using different materials coupled together. (b) On-chip integration. Different materials co-exist on a single chip.

2.2 Chip-to-chip integration

There are a few reports for chip to chip integration using silica and polymer PLC chips. One application is tunable optical dispersion compensator[2] (TODC) and another is reconfigurable add/drop multiplexer[3] (ROADM). In both cases, polymer is used to realize lower power consumption for functions such as lens, attenuators, or switches, and silica is used to realize lower propagation loss for routing, and wavelength filters. Besides polymer/silica materials, recently chip-to-chip integration is used frequently to realize coherence transceivers[4]. The concept is same for this material combination too. For modulators, lithium niobate is used to achieve faster modulation speed and silica is used to utilize its lower loss characteristics.

2.3 Example of chip-to-chip integration

As an example of chip-to-chip integration, we built a tunable optical dispersion compensator (TODC) using a silica PLC and a polymer chip. The silica chip contains an arrayed waveguide grating (AWG) structure. Then a polymer chip as a thermo-optical lens is attached. By applying the power to the heater array on the polymer chip this hybrid system obtains tunability in optical dispersion compensation.

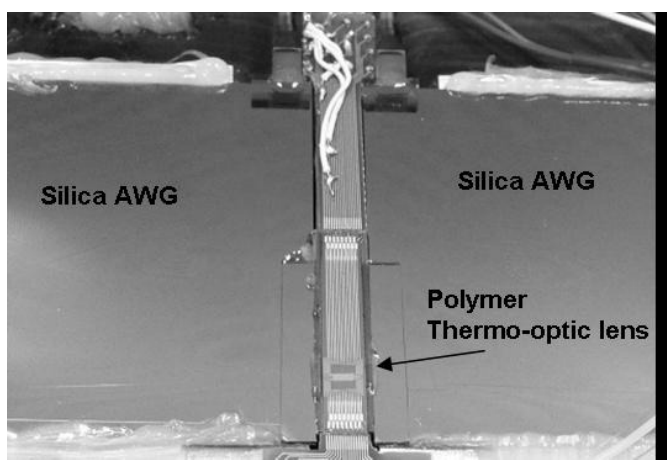

Figure 2. A photograph of silica/polymer hybrid TODC. An example of chip-to-chip integration.

Benefits of hybridization here are the lower power consumption, higher reliability, wider tuning range, and lower cost. The monolithic version of this device requires very high power for tuning. For example, it is reported[2] that it required ~7W to tune over 400 ps/nm for a silica monolithic device. The high power requirement is due to the lower index tuning capability of silica material, i.e. smaller thermo-optic (TO) coefficient. High power requirement possibly leads to many challenges in practical devices. For example, heat management of the device can be problematic since a small device consuming >7W can generate a large amount of heat and increases the local temperature significantly. The extreme temperature around heaters also raises the reliability concern of the heater structure. Using a polymer chip as a thermo-optical lens, we can lower the power consumption since polymer's TO coefficient is ~30 times larger than silica's.

A photograph of the assembled device is shown in Fig. 2. It contains two AWG chips at the both side of a polymer thermo-optical lens chip. The measured performance is shown in figure 3. Using polymer chip as the thermo-optical lens, this device operates with the power consumption at polymer chip down to ~100mW for tuning over ~1200ps/nm.

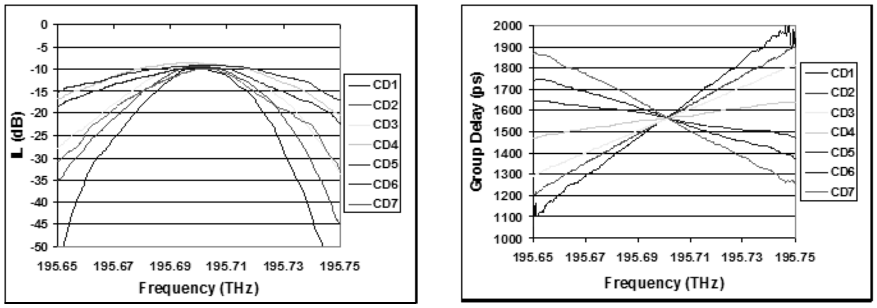

Figure 3. Measured test results of silica/polymer hybrid TODC. Seven different settings for thermo-optical lens are shown.

2.4 On-chip integration

For on-chip integration methods, polymer and silica materials co-exist on a single chip surface. Various hybrid structures have been reported. Since polymer can be processed using the compatible silica processes such as spin coating, photo lithography, UV curing, RIE, etc., polymer is readily applied in different structures. Some of the reported silica/polymer structures are shown in Fig. 4. Polymer can fill the gap created between silica waveguides[5, 6] (a). Polymer can be used as both core and top clad[7], or as only clad[8, 9] for waveguide structures (c, d). Some applications use a slab guide structure[10] (b). Functions realized by these structures include athermal AWG[5, 6], variable optical attenuators[8,9], couplers[8], optical switches[7], and optical scanners[10]. Many of these applications utilize polymer's negative thermo-optic coefficient to tune the refractive index in the opposite direction of silica. Namely, refractive index and thermo-optic coefficient are important parameters to consider for the device design. The propagation loss is another key parameter. Optical polymer's physical constants, around wavelength of 1550nm, are listed in the table 1. Enablence's hyper-linked fluoropolymer (EP polymer) has both a large TO coefficient and low propagation loss that makes it preferable choice for optical network device applications. As more practical aspects of EP polymer, EP polymer can be spin coated and UV photo lithographed on to silica/silicon or other material surfaces. EP polymer is also established as reliable optical material for volume production of polymer based PLC devices[18, 19].

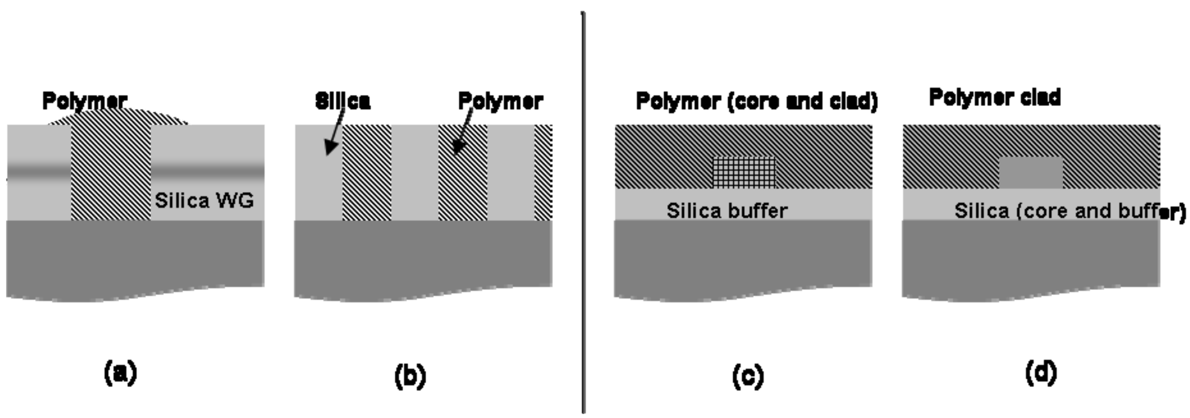

Figure 4. Schematic diagrams of on-chip hybrid integration of polymer and silica. (a) and (b) are side views. (a) Polymer fills the gap between silica waveguides. (b) Slab structure with silica and polymer. (c) Polymer waveguide core and top clad on a silica buffer layer. (d) Silica waveguide core and buffer with polymer clad.

2.5 Example of on-chip integration

Popular use of optical polymer in on-chip integration application is athermalization. For example, AWG can be athermalized, i.e. no spectral shift with temperature changes, by utilizing polymer's negative thermo-optic coefficient. Many designs of this application have been proposed with different waveguide structures or polymer trench locations[5, 6].

Here, we present an example, an athermal ring resonator in silicon waveguides, we demonstrated in a recent report[15]. Please note that this example uses a-Si waveguide, not silica. Recent multi-core design of electronic chips demands large capacity communication on a chip. Due to seamless integration capability in CMOS processes and recent advances, silicon photonics is the natural choice for electronic/photonic integration platform. However, one of the issues of this material, especially used as WDM system, is that silicon waveguide's effective index is sensitive to temperature changes so that the resonant wavelength shifts in devices such as wavelength filters. We applied athermalization technique using polymer material for a silicon ring resonator.

For the athermalization application, as discussed in previous section, thermo-optic coefficient of polymer should be comparable to the one to be canceled. In our case, since the waveguide core is silicon, dn/dT ~1.8×10^{-4} K^{-1}, a polymer with the larger TO coefficient is required. The refractive index of the polymer determines the effective index, and the confinement factor of waveguides, this also affects the efficiency of dn/dT compensation. The loss of the material is important, but bend loss could be dominant for this design. Again from the table 1., Enablence's hyperlinked fluoro-polymer has desirable characteristics for a-Si waveguide circuit athermalization.

Table 1. Physical constants of optical polymers and other optical materials, at ~1550 nm wavelength.

Material	Loss (dB/cm)	Refractive index	T/O Coef. dn/dT (10^{-4} K^{-1})	Note
Enablence polymer	0.1	1.4	-2.7	Hyperlinked fluoro-polymer
Optical silicone	0.7	1.5	-3.6	Dimethylsiloxane, Ref [11]
PMMA	1.5	1.5	-1.2	Ref [12]
Fluorinated polyimides	1.0	1.6	-0.1	Ref [13, 14]
Silica	0.1	1.5	0.1	
Silicon	0.1	3.5	1.8	

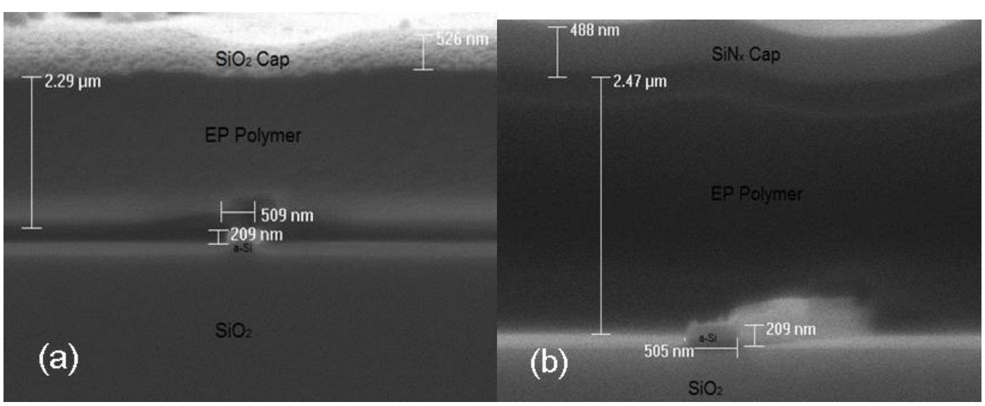

Figure 5. Photographs of a-Si/Polymer/dielectric layered structures. (a) On top of Enablence polymer layer, silicon dioxide layer is deposited. (b) On top of Enablence polymer layer, silicon nitride layer is deposited. From Ref [16].

In the report[15], athermal a-Si ring resonators is demonstrated. Waveguide dimension used is 700nm x 206 nm. 3 microns thick EP polymer cladding layer is spin coated and cured. The shift of resonant wavelength was measured as low as 0.5 pm/K. In another report[16], we also demonstrated deposition of a dielectric layer on top of the polymer cladding layer. By choosing the thermal profile of the processes carefully, ~0.5 micron of SiO_2 or SiN_x layer was successfully deposited on top of the polymer layer by high density plasma chemical vapor deposition, Fig. 5. The device performance was not affected by the dielectric layer deposition. Now, the dielectric layer can protect the polymer layer from severe conditions in other processes. This suggests the possible use of the silicon/polymer platform with CMOS technology to integrate further layers of electronics/photonics.

3. SILICA PLC HYBRIDIZATION

In this section, we discuss another type of material platform for hybridization which is silica PLC. We developed integration methods to add active components directly on top of silica PLC chips[17]. This allows us to reduce the cost and the size of devices and to optimize the performance. These benefits of integration come from following reasons. The total device size is reduced, since we mount active components directly on the chip. There is no need for fiber connections, alignment supports, separate packaging. The cost reduction is due to the material cost, manufacturing cost, and channel number scaling advantage. Automatic nature of the assembly process reduces the manufacturing cost significantly and also reduces the lead time. And the cost increase for higher channel count device is minimal compared to, for example, micro-optics assembly. The performance enhancement is also one of the benefits of hybrid integration. Since we can optimize the passive PLC and active components performance independently, the combined system performance is also optimized. In contrast, monolithic integration often requires compromised performances in both PLC and active components to use a single material platform or compatible materials.

In our integration design, we fully utilize the silica PLC's capability. Conventionally, for hybrid integration, the base waveguide circuits could be merely connections between components mounted on top. In our system, the silica PLC includes functional components as well as design features for integration. This way, the hybridized system can have unique functionality additional to cost benefits. Examples of such PLC functions are splitter, arrayed waveguide grating, and mirrors. To achieve automatic assembly of the system, we also added features for integration such as alignment marks for PD, and LD mounting. For PD, 45 degree mirrors are integrated as a part of the silica PLC, Fig. 6 (a). For LD, a deep pit with pedestal is fabricated in the silica PLC. This pedestal allow the precise vertical alignment, then the mounting solder fills the gap outside of the pedestal so that the vertical alignment won't be affected, Fig. 6 (b).

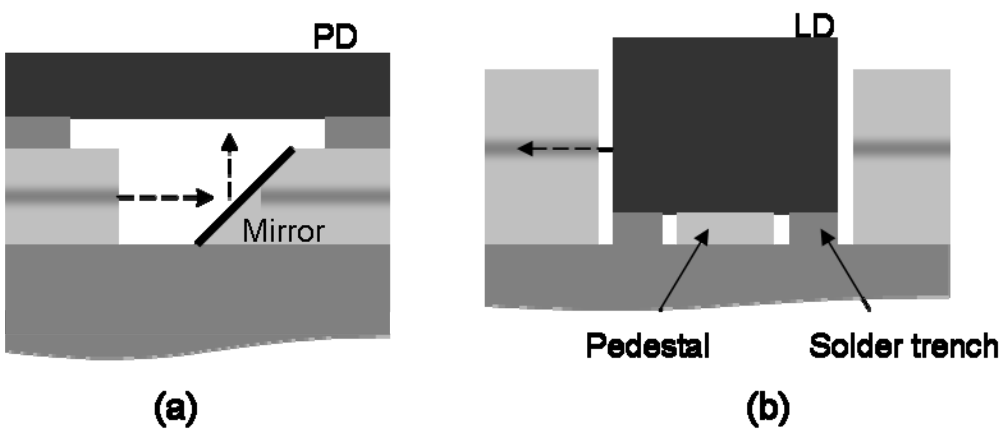

Figure 6. Schematic diagrams of features for hybrid integration on silica PLC. (a) The integrated 45 degree mirrors are used to couple lightwave signal from PLC waveguides to PDs. (b) The mounting pit is used to integrate LDs.

Here are two examples of silica PLC hybridization at Enablence. Figure 7 shows a triplexer chip for FTTH application. The chip includes a wavelength filter grating in PLC layer. PDs and electronic components mounted on top are visible. Using hybrid integration, this chip achieved a competitive price in the cost-conscious, FTTH market. Figure 8 shows an example of even higher level of integration that is a 10x10G receiver chip. This chip includes arrayed waveguide grating based WDM filter, integrated mirrors for PD coupling, and alignment marks in silica PLC layer. PDs and electronics such as capacitors and transimpedence amplifiers are mounted in automatic fashion. Because of the high level integration, this device in a fully packaged form has the foot print of approximately 40 x 30 x 10mm. This extremely small size is only possible with hybrid integration.

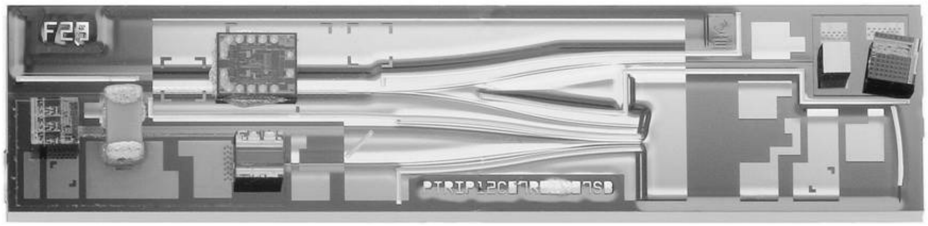

Figure 7. A photograph of a triplexer chip realized by hybrid integration of silica PLC and active components.

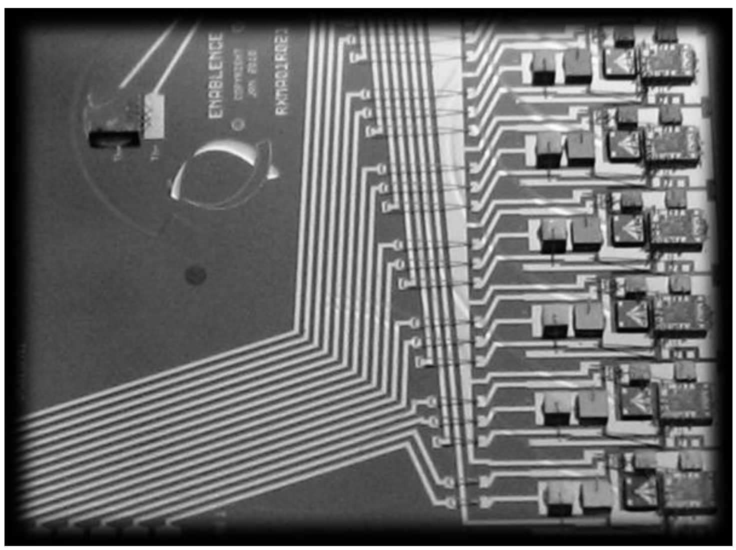

Figure 8. A highly integrated 10x10G receiver chip (part).

4. CONCLUSION

We reviewed the hybrid integration of polymer and silica PLCs using two categories, chip-to-chip and on-chip. An example of each type is used to discuss the benefits of integration. Silica PLC hybrid integration is also discussed. It is clear that hybrid integration can achieve higher performances at lower cost. We believe that more applications will be realized by these methods in the future.

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REFERENCES

[1] "Visual networking index" Cisco Systems, <http://www.cisco.com/en/US/netsol/ns827/networking_solutions_sub_solution.html> (2013).
[2] Doerr, C. R., Blum, R., Buhl, L. L., Cappuzzo, M. A., Chen, E. Y., Wong-Foy, A., Gomez, L. T., and Bulthuis, H., "Colorless tunable optical dispersion compensator based on a silica arrayed-waveguide grating and a polymer thermooptic lens," IEEE Photonics Technology Letters 18(11), 1222-1224 (2006).
[3] Radojevic, A., Fujita, J., Gerhardt, R., Izuhara, T., and Eldada, L., "Hybrid-integrated ROADM for reconfigurable optical networks," Proc. European Conference on optical communication 30, Tu11.4.5 (2004).
[4] Goh, T., Yamazaki, H., Kominato, T., Mino, S., "Novel flexible-format optical modulator with selectable combinations of carrier numbers and modulation levels based on silica-PLC and $LiNbO_3$ hybrid integration" Proc. OFC, OWV2 (2011).
[5] Kamei, S., Inoue, Y., Shibata, T., and Kaneko, A., "Low-loss and compact silica-based athermal arrayed waveguide grating using resin-filled groove," Journal of Lightwave Technology 27(17), 3790-3799 (2009).
[6] Kokubun, Y., Funato, N., and Takizawa, M., "Athermal waveguides for temperature-independent lightwave devices," Photonics Technology Letters 5(11), 1297-1300 (1993).
[7] Yeo, DM., and Shin, SY., "Polymer-silica hybrid 1x2 thermooptic switch with low crosstalk," Optics Communications 267(2), 388-393 (2006).
[8] Zhang, Z., Xiao, G. Z., Zhao, P., and Grover, C. P., "Planar waveguide-based silica-polymer hybrid variable optical attenuator and its associated polymers," Applied Optics 44(12), 2402-2408 (2005).
[9] Bosc, D., Devoldere, N., Bonnel, M., Favennec, J.L., and Pavy, D., "Hybrid silica polymer structure for integrated optical waveguides with new potentialities," Materials Science and Engineering: B 57(2), 155-160 (1999).
[10] Tang, S., Li, B., Han, X., Taboada, J.M., Jang, CH., Kin, JH., Sun, L., and Chen, R.T., "An integrated thin-film thermo-optic waveguide beam deflector," Applied Physics Letters 76(16), 2289-2291 (2000).
[11] Norris, A., et al., "High Reliability of silicone materials for use as polymer waveguides," Proc. SPIE Linear and Nonlinear Optics of Organic Materials III 5212, 76-82 (2003).
[12] Wunderlich, W., "Physical constants for Poly(methyl methacrylate)", *Polymer Handbook, 3rd ed.*, Brandrup, J. and Immergut, E.H., V77-V80, Wiley, New York, 1989.
[13] Ando, S., "Optical properties of fluorinated polyimides and their applications to optical components and waveguide circuits," Journal of Photopolymers Science and Technology 17(2), 219-232 (2004).
[14] Ma, H., Jen, A. K. –Y., Dalton, L. R., "Polymer-based optical waveguides: materials, processing, and devices," Adv. Mater. 14(19), 1339-1365 (2002).
[15] Raghunathan, V., Ye, W.N., Hu, J., Izuhara, T., Michel, J. and Kimerling, L., "Athermal operation of silicon waveguides: spectral, second order and footprint dependencies." Optical Express 18(17), 17631-17639 (2010).
[16] Raghunathan, V., Izuhara, T., Michel, J. Kimerling, L., "Stability of polymer-dielectric bi-layers for athermal silicon photonics," Optics Express 20(14), 16059-16066 (2012).
[17] Pearson, M., Bidnyk, S., and Balakrishnan, A., "The evolution and commercialization of large scale photonic circuits," International conference on information photonics, 1-2 (2011).
[18] Eldada, L., "Polymer integrated optics: promise vs. practicality," Proc. SPIE 4642, 11-22 (2002).
[19] Fujita, J., Izuhara, T., Radojevic, A.M., Gerhardt, R., and Eldada, L., "32-channel reconfigurable optical add/drop multiplexer on a chip," Proc. SPIE 5729, 130-138 (2005).